Nanoelectronic Device Technology

IEEE EDS WIMNACT 23

@Heritage Institute of Technology

April 9, 2010

Frontier Research Center

Tokyo Institute of Technology

Hiroshi Iwai

Tokyo Institute of Technology

Founded in 1881, Promoted to Univ. 1929

Institute Overview

Einstein Visit

Established in 1881→ 130th anniversary in 2011

3 undergraduate schools

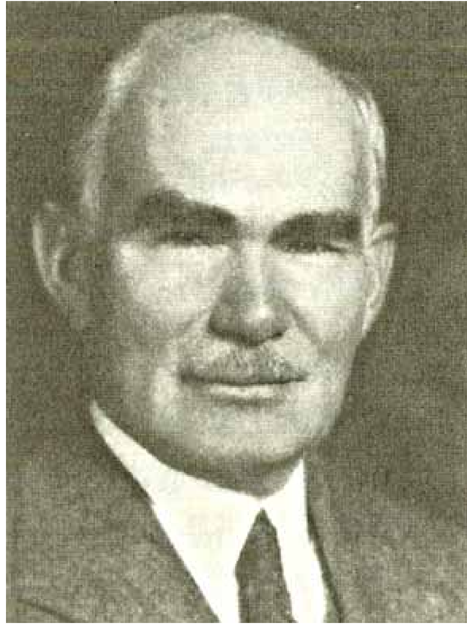
School of Science, School of Engineering, School of Bioscience and Biotechnology

7 graduate schools

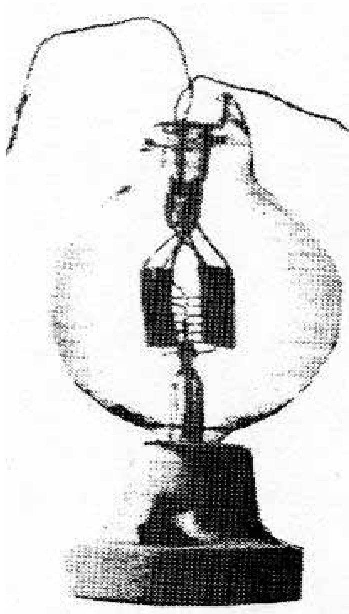
Science and Engineering Science, Science and Engineering Technology,
Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

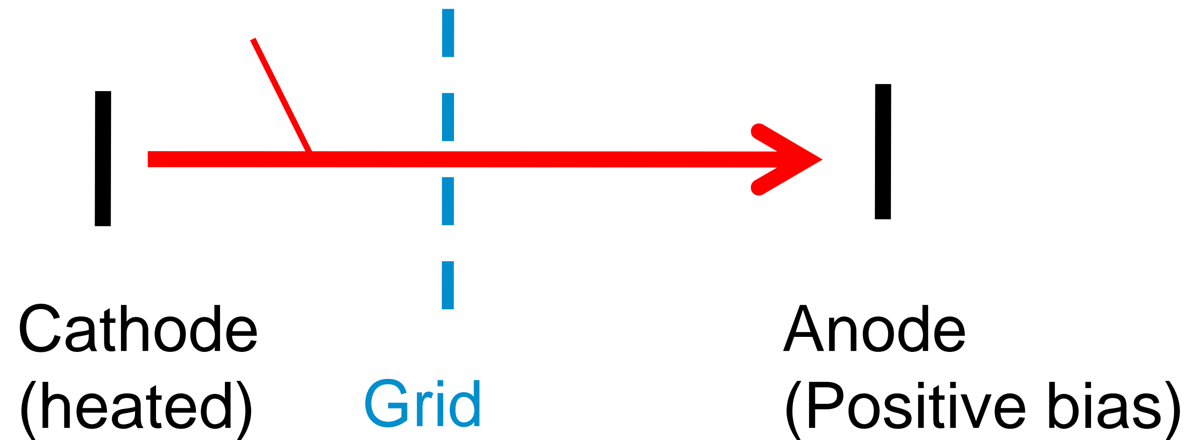
	Undergraduate	Graduate	Master's	Doctoral	Teaching Staff	Student/Instructor	Staff
Tokyo Inst.	**5,000**	**5,000**	**3,500**	**1,500**	**1,200**	**8.3**	**550**
Per Year	**1,200**		**1,800**	**500**			



Lee De Forest

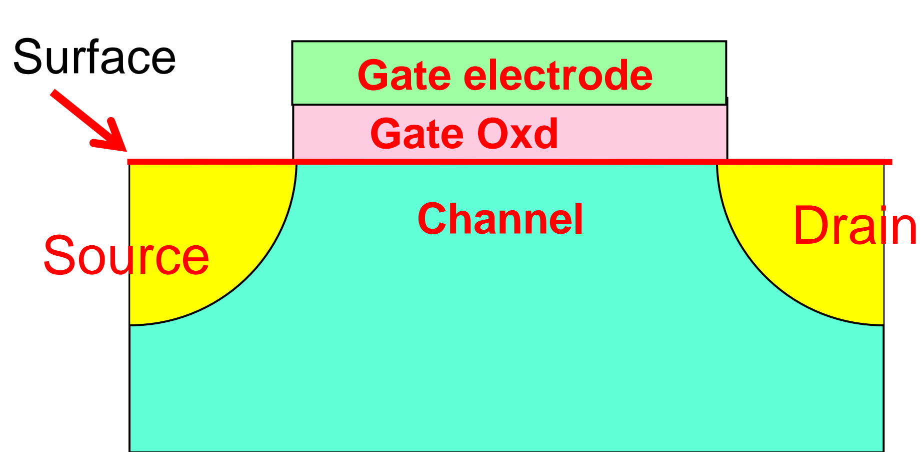


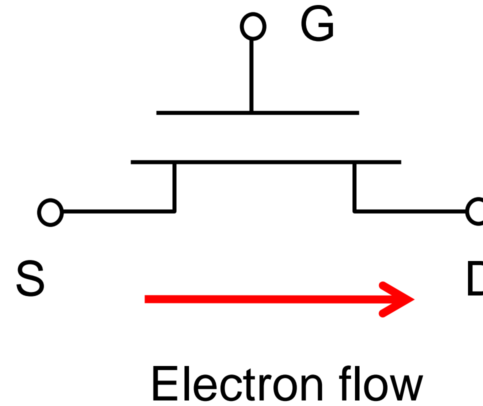
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906



Same mechanism as that of transistor

Today's transistor: MOSFET for CMOS LSI

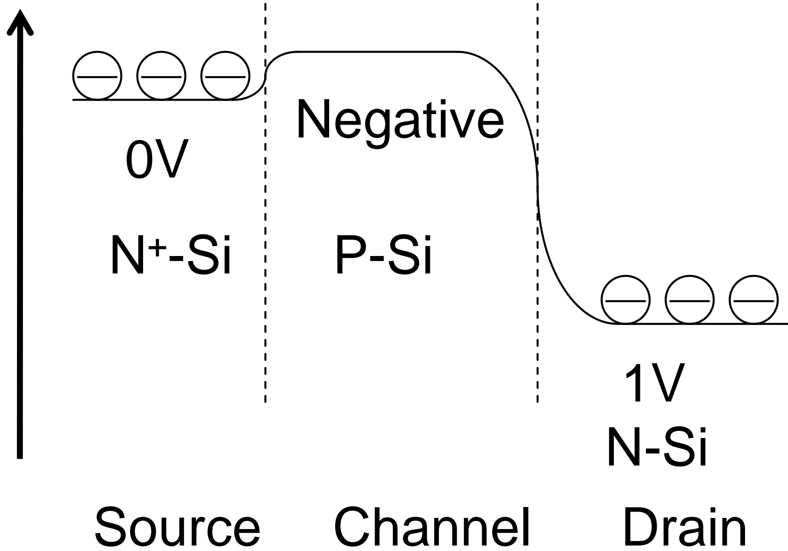


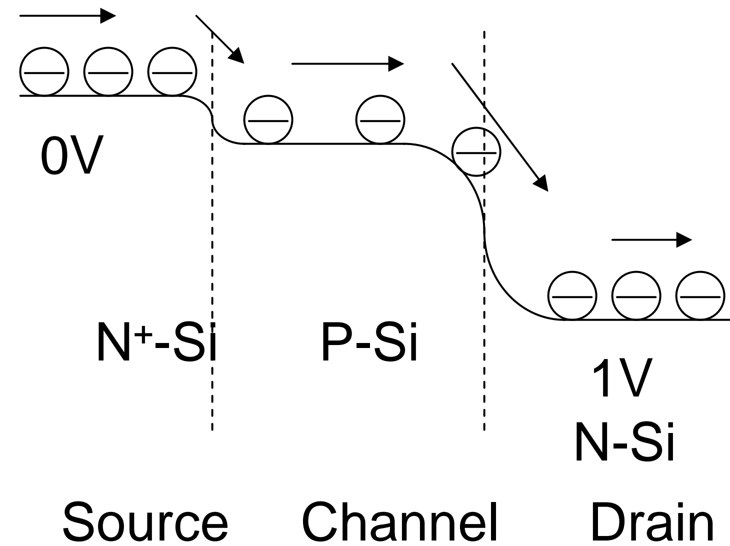


0 bias for gate

Positive bias for gate

Surface Potential (Negative direction)





Gate Electrode
Poly Si

Gate Insulator
SiO_2

Substrate
Si

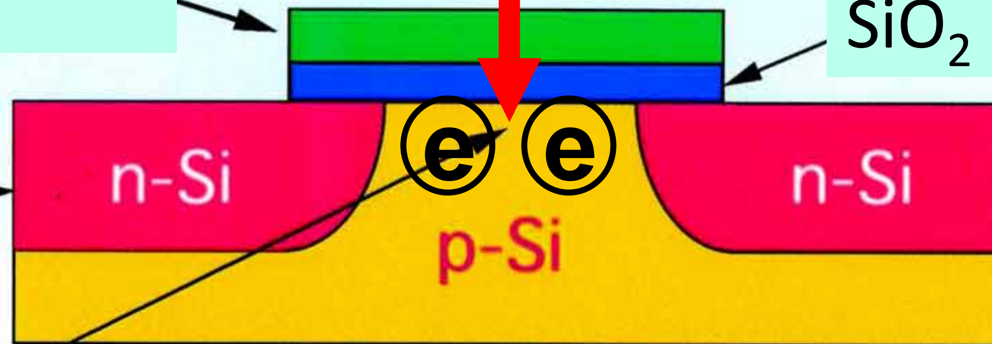
MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching

Gate Electrode
Poly Si

Gate Insulator
SiO_2

Source



Drain

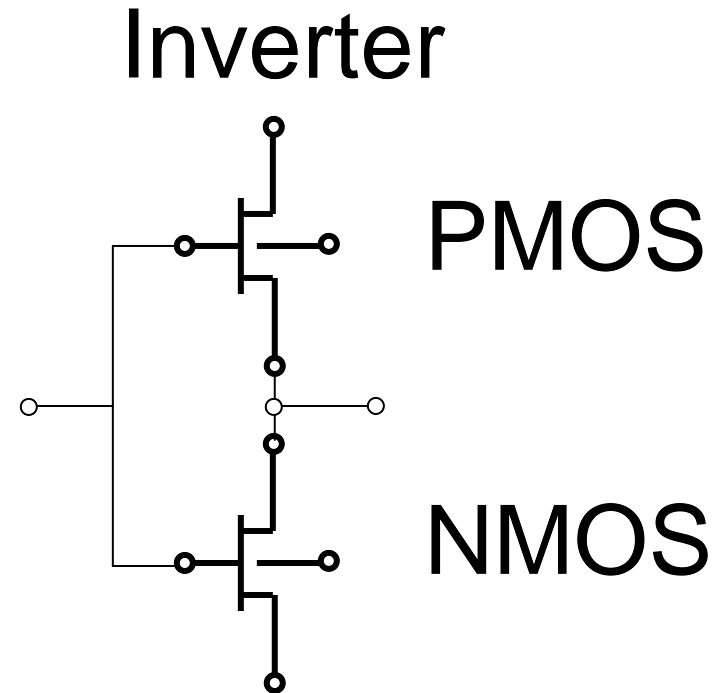
Si
Substrate

Channel

N-MOS (N-type MOSFET)

CMOS

Complimentary MOS



When NMOS is ON, PMOS is OFF

When PMOS is ON, NMOS is OFF

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

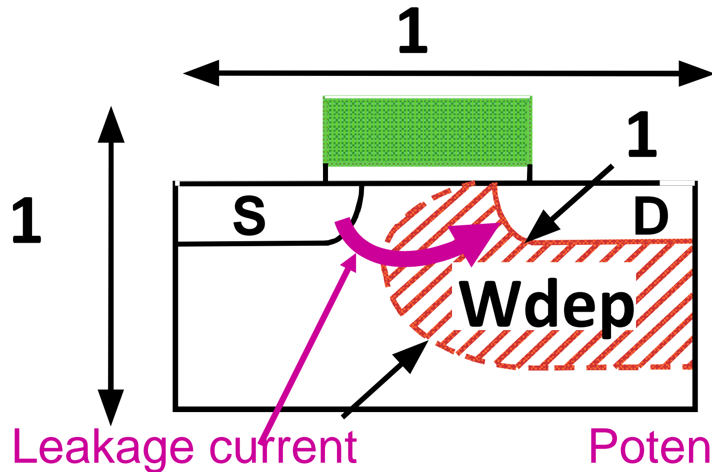
→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

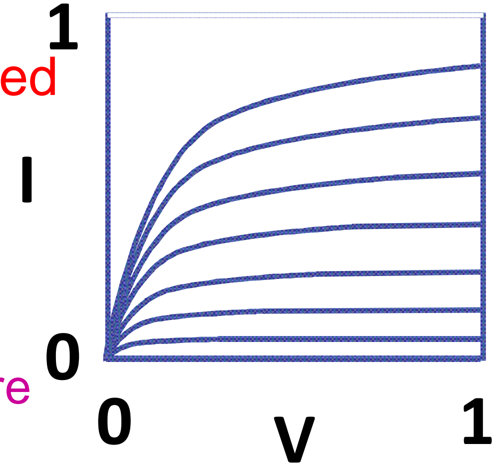
Thus, downsizing of Si devices is the most important and critical issue.

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

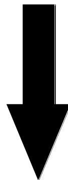
Wdep has to be suppressed
Otherwise, large leakage between S and D



Leakage current

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

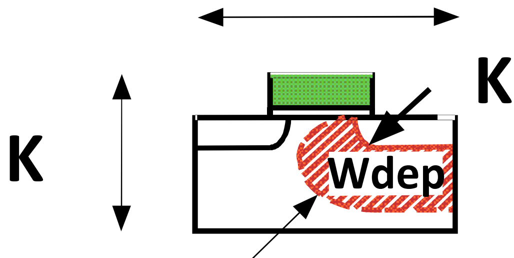
K=0.7 for example



X , Y , Z : K, V : K, Na : 1/K

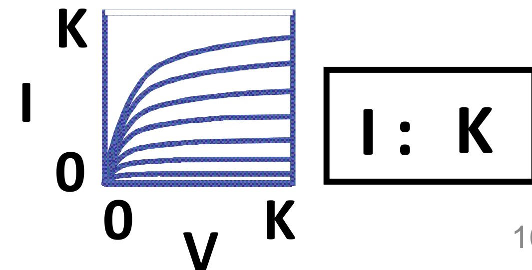
By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$Wdep \propto \sqrt{V/Na}$$

: K



I : K

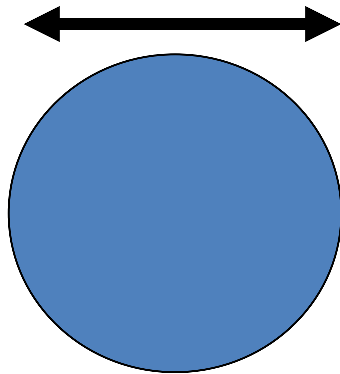
Every 3 years: k= 0.7	6 Years:k= 0.7^2 =0.5
Single MOFET	
Vdd → 0.7	Vdd → 0.5
Lg → 0.7	Lg → 0.5
Id → 0.7	Id → 0.5
Cg → 0.7	Cg → 0.5
P (Power)/Clock → $0.7^3 = 0.34$	P (Power)/Clock → $0.5^3 = 0.125$
τ (Switching time) → 0.7	τ (Switching time) → 0.5
Chip	
N (# of Tr) → $1/0.7^2 = 2$	N (# of Tr) → $1/0.5^2 = 4$
f (Clock) → 1/0.7 = 1.4	f (Clock) → 1/0.5 = 2
P (Power) → 1	P (Power) → 1

Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Electron wave length

10 nm



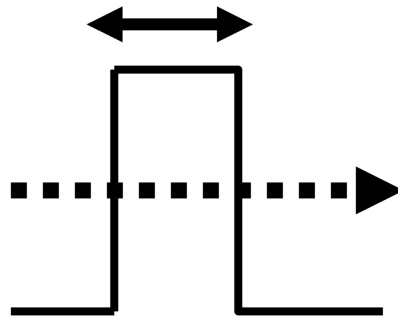
Downsizing limit!

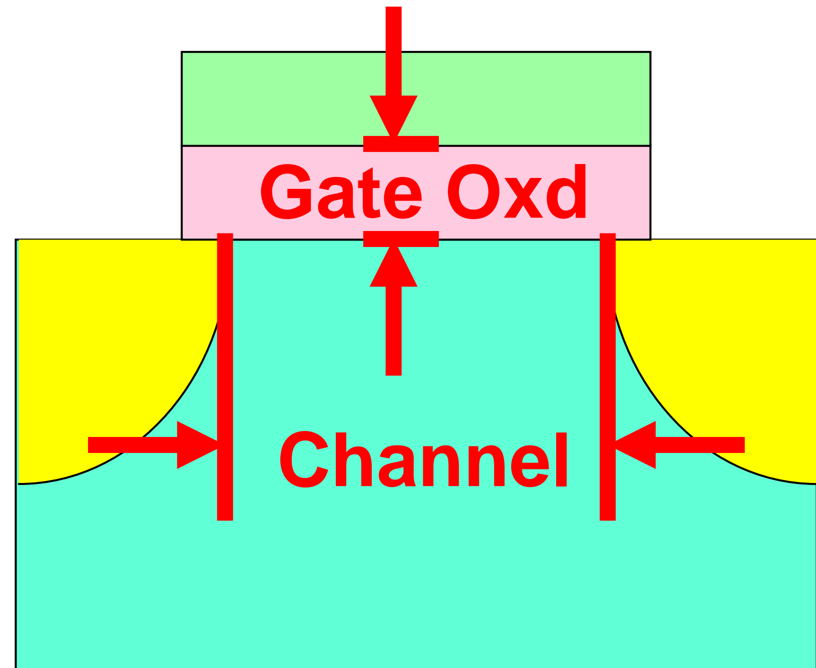
Channel length

Gate oxide thickness

Tunneling distance

3 nm

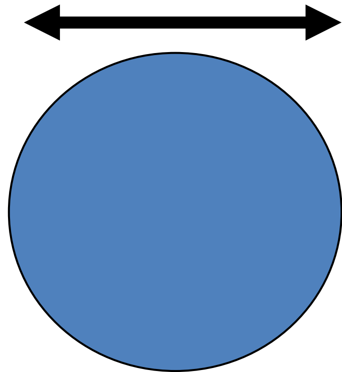




Prediction now!

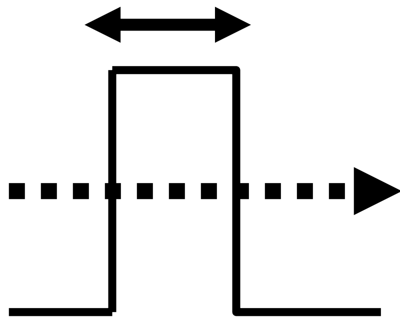
Electron wave length

10 nm



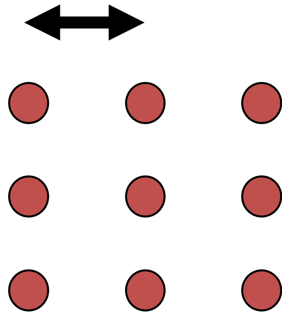
Tunneling distance

3 nm



Atom distance

0.3 nm



MOSFET operation

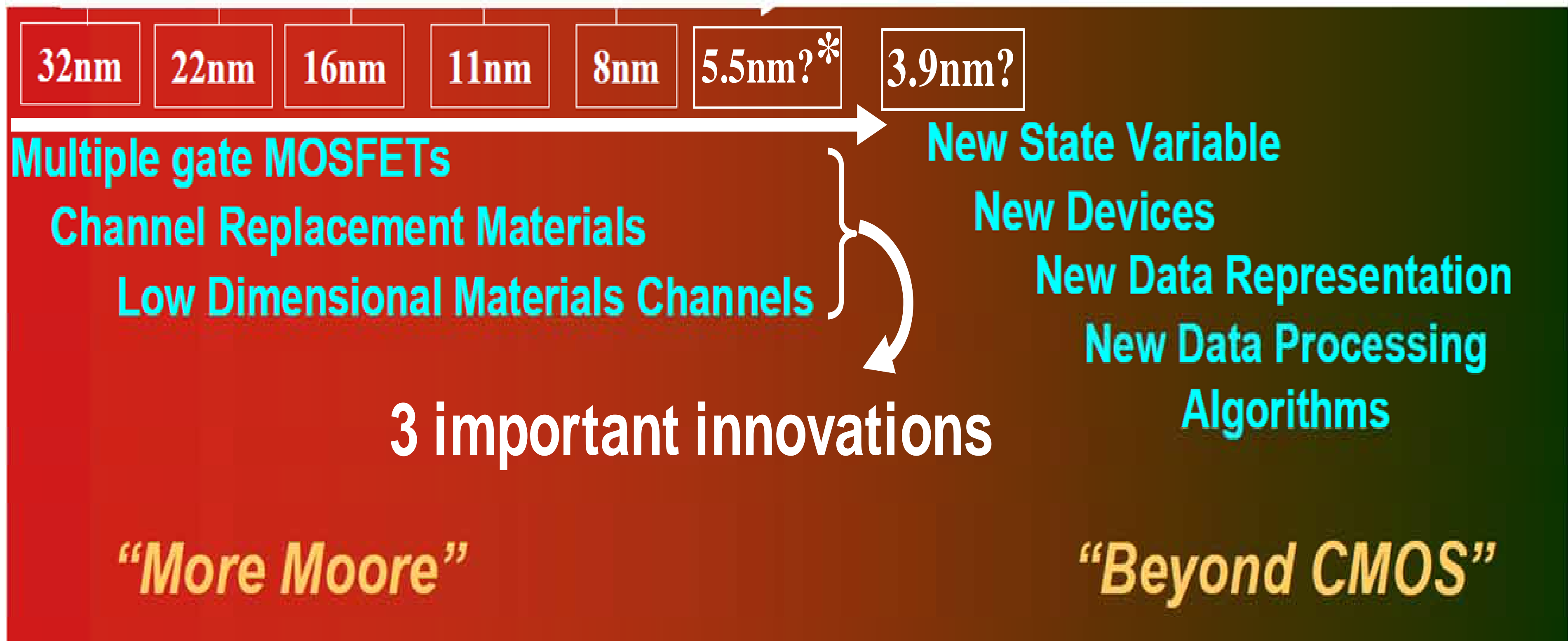
Lg = 3 nm?

Below this, no one knows future!

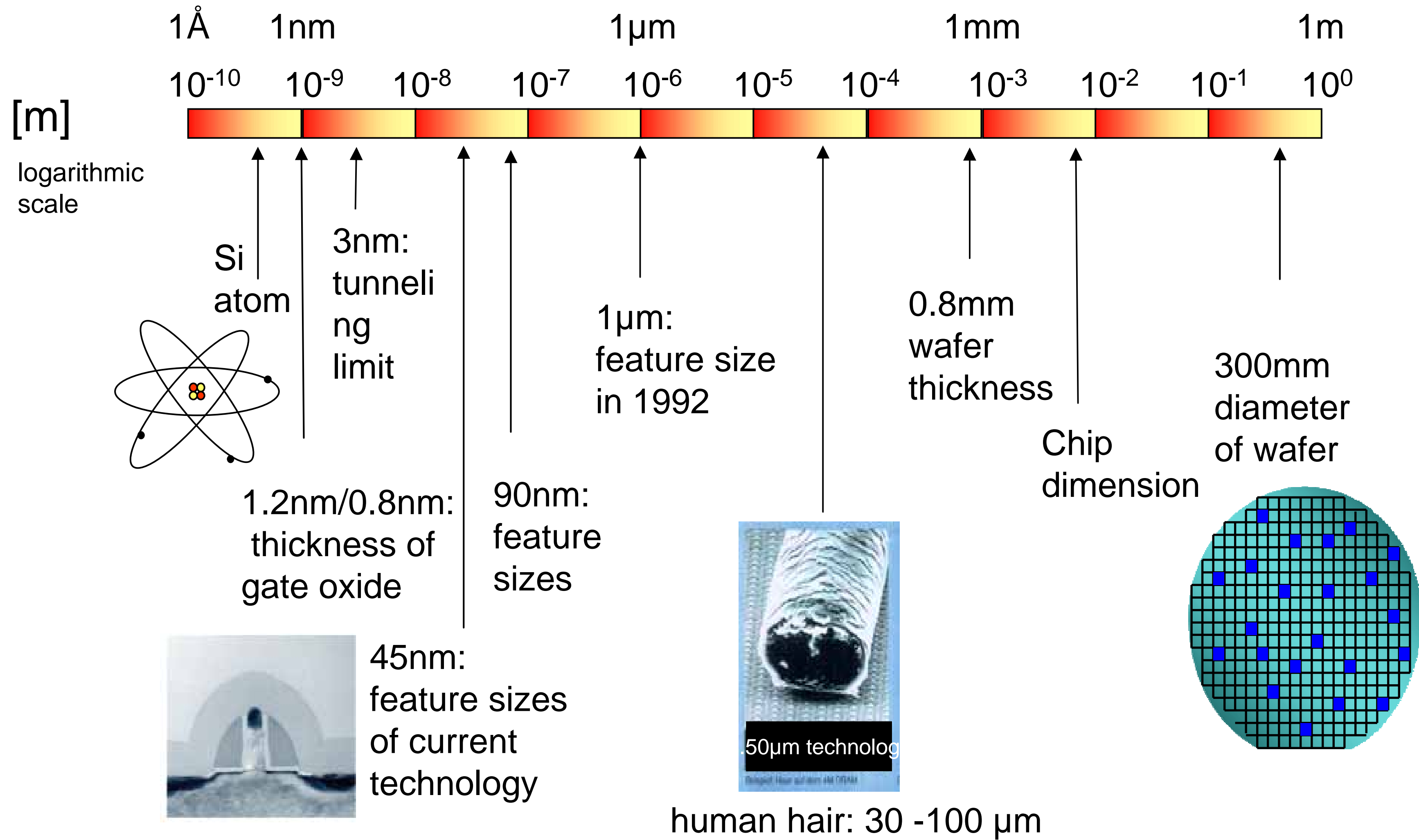
-Two candidates have emerged for R & D

1. Nanowire/tube MOSFETs
2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.



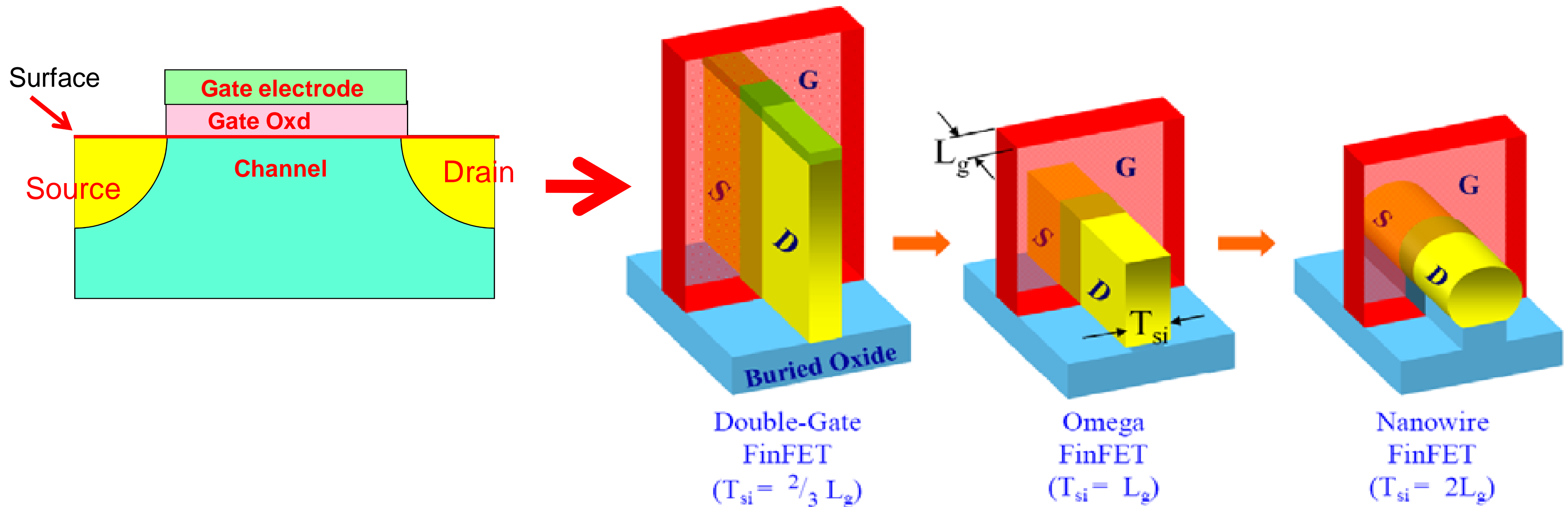
Semiconductor Technology - Length Scales

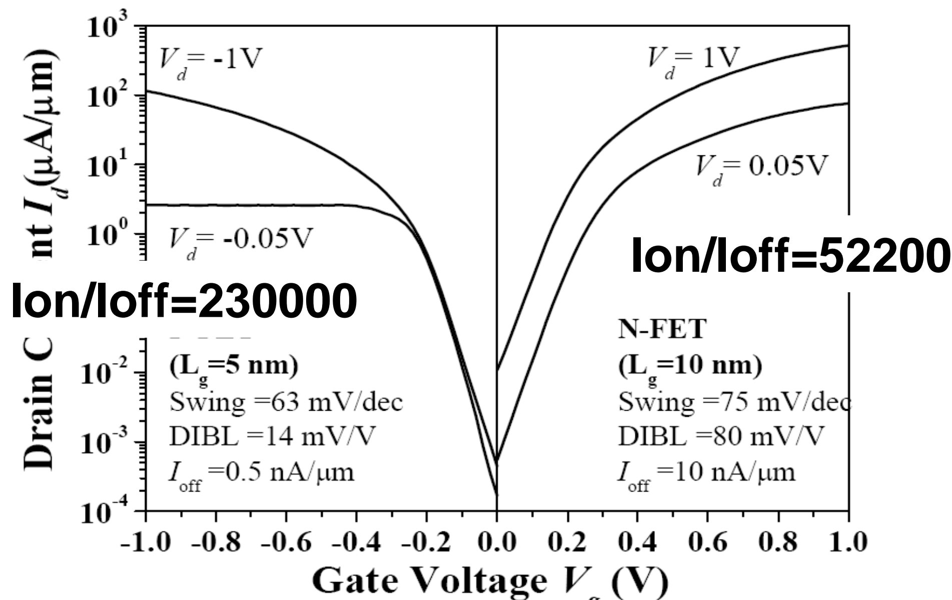


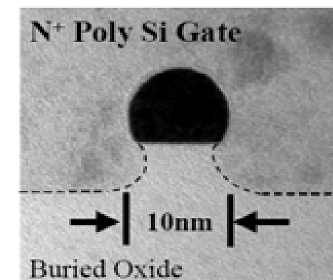
(source : European Nanotechnology consortium)

Courtesy of M.K. Radhakrishnan

FinFET to Nanowire







Channel conductance is well controlled by Gate even at L=5nm

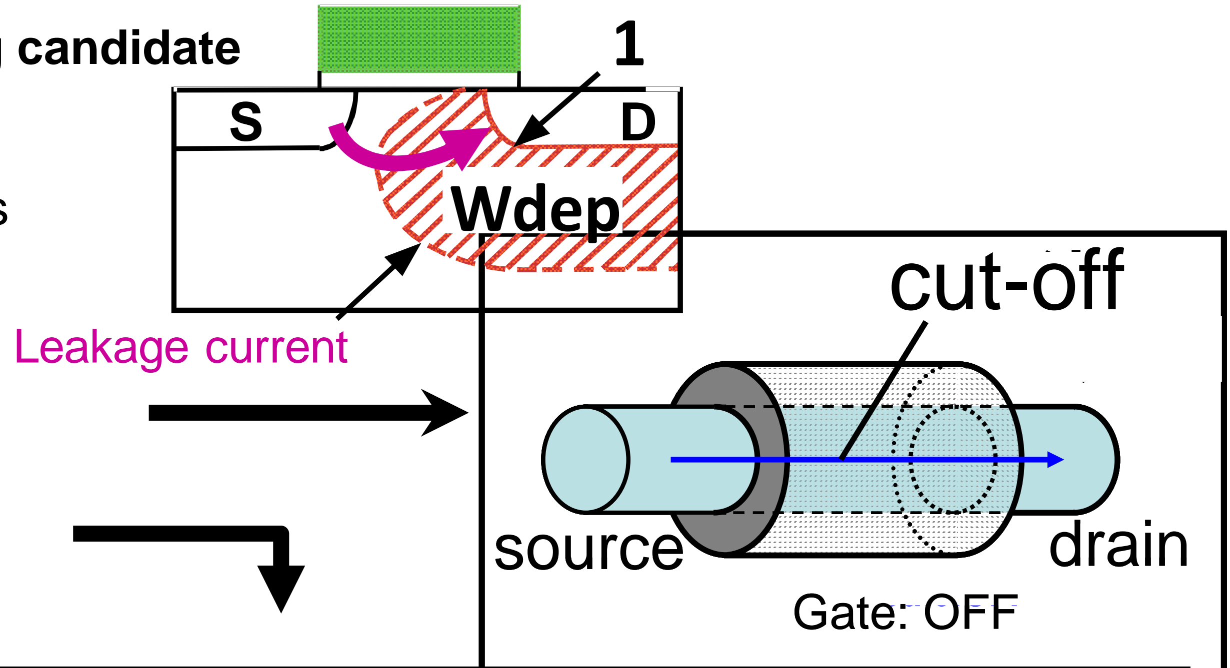
F.-L.Yang, VLSI2004

Si nanowire FET as a strong candidate

1. Compatibility with
   current CMOS process

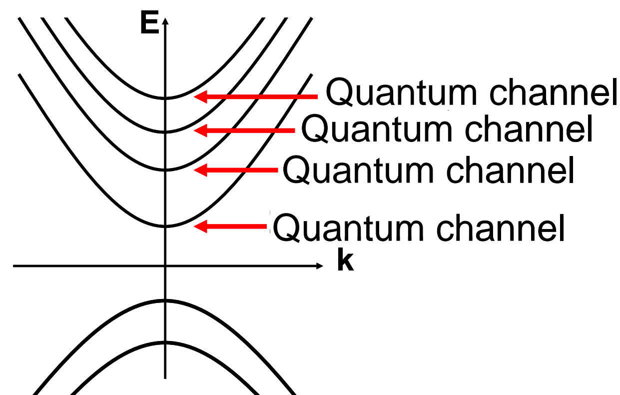
2. Good controllability of I_{OFF}

3. High drive current

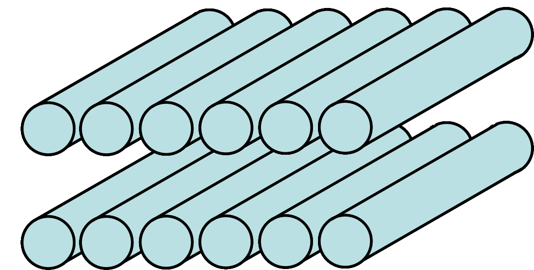


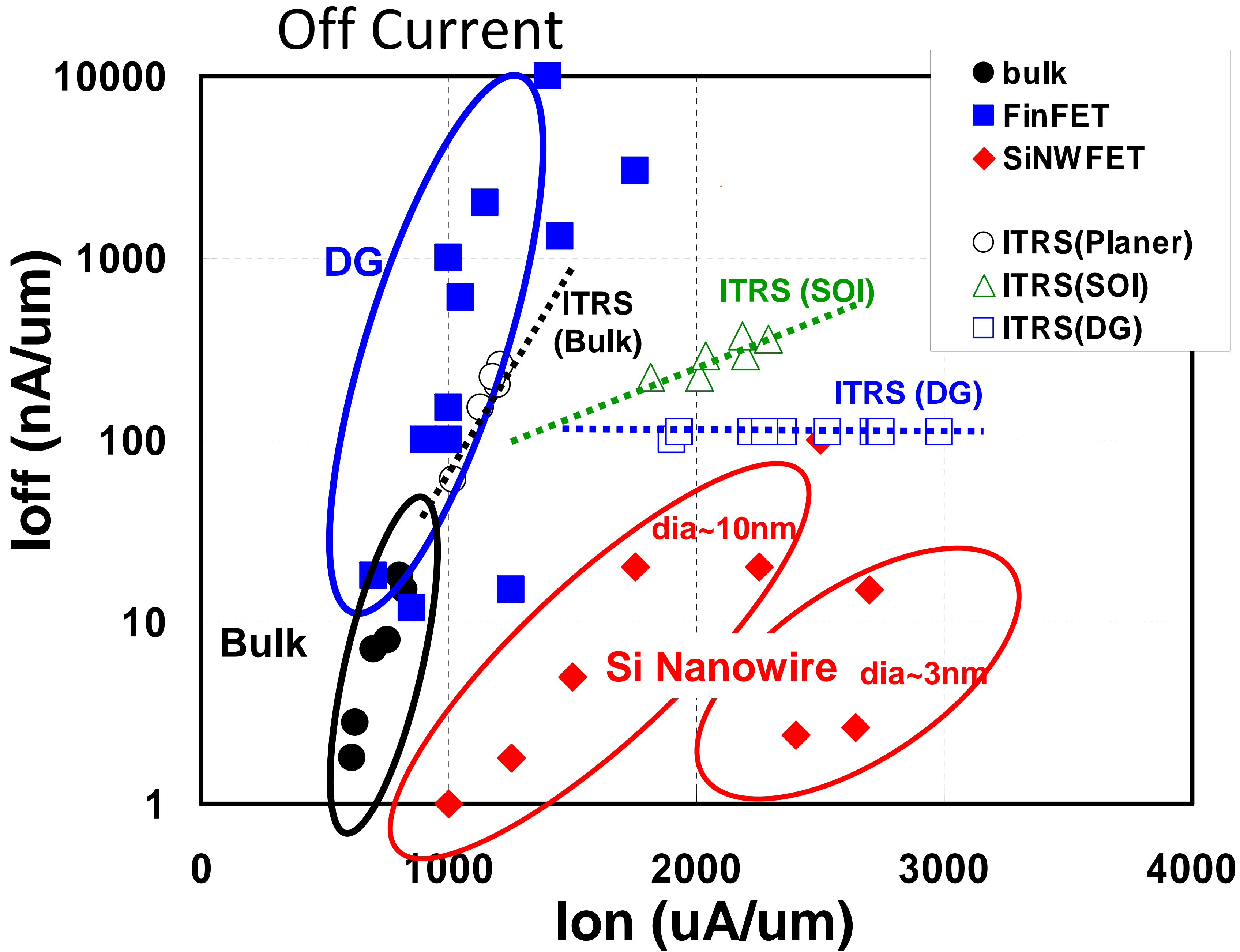
1D ballistic conduction

Multi quantum Channel



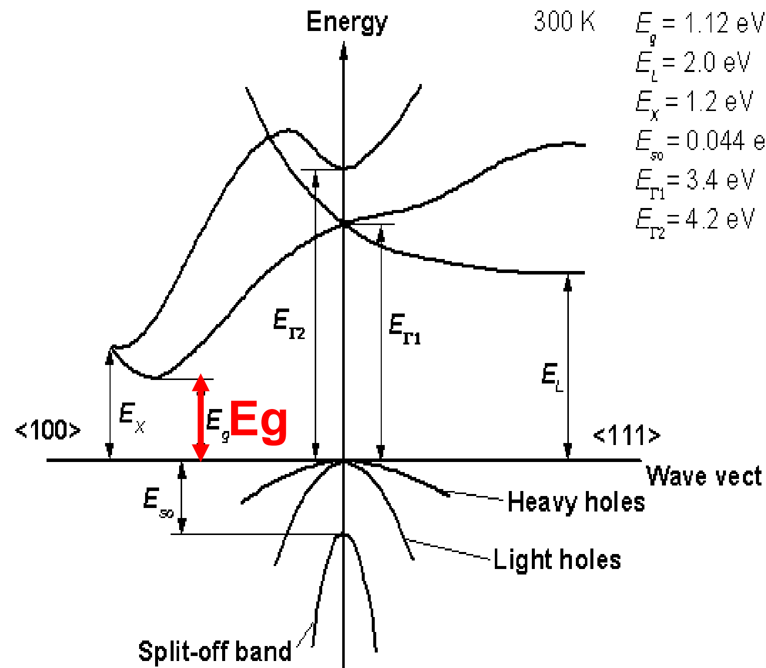
High integration of wires



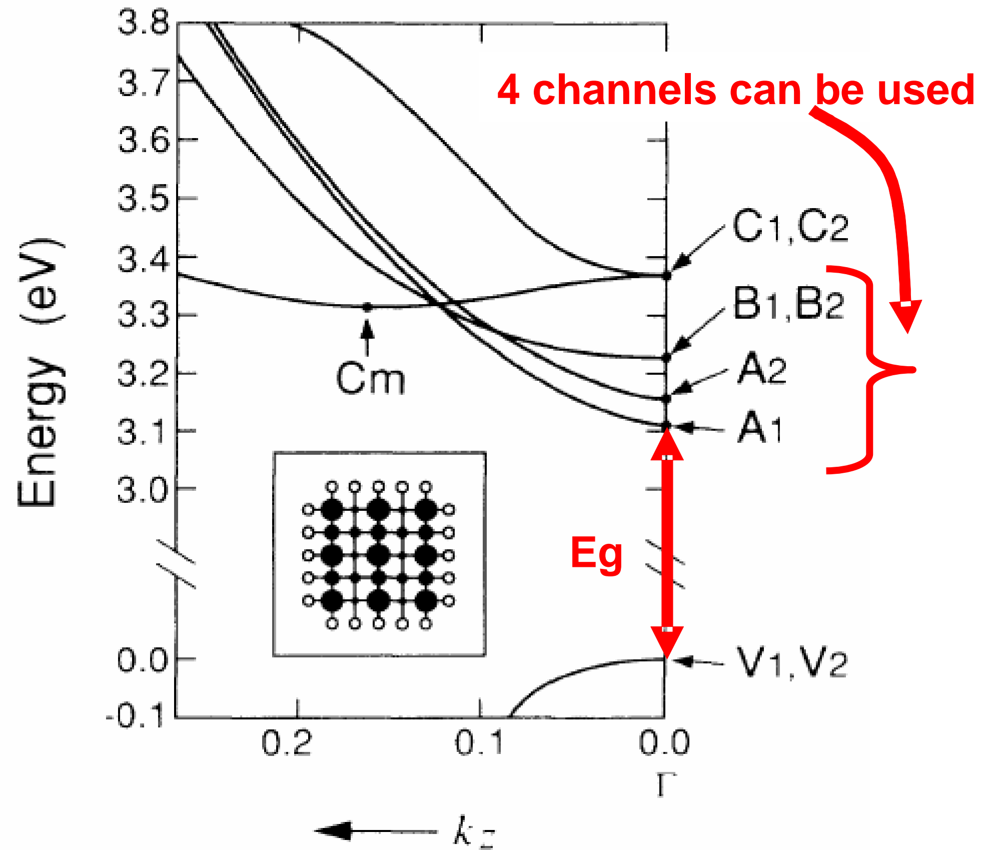

Off Current
10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



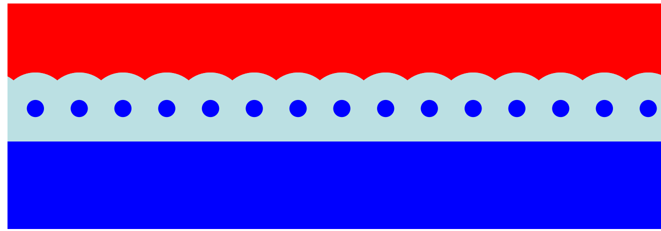
Energy band of Bulk Si



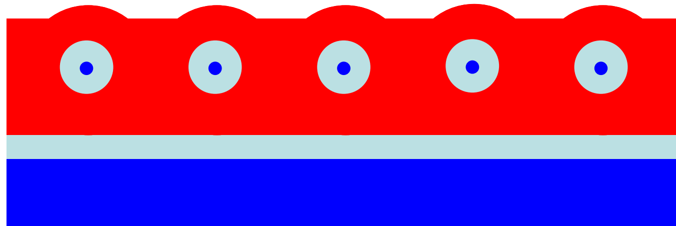
Energy band of 3 x 3 Si wire

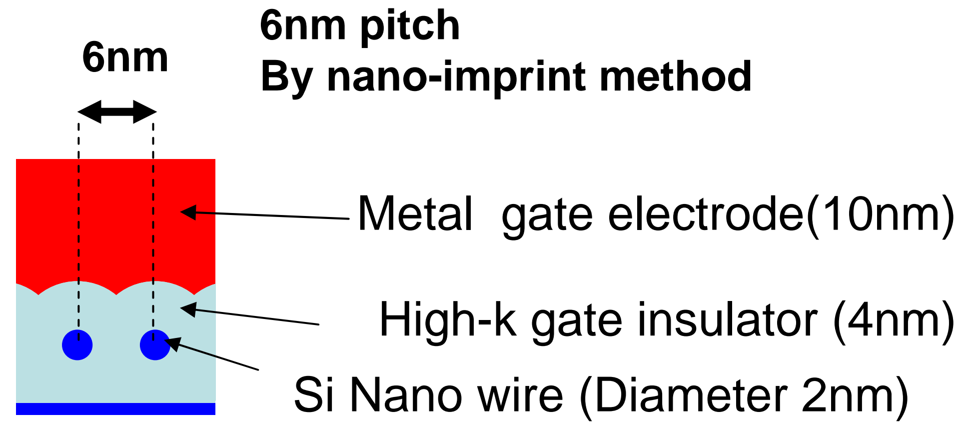
Maximum number of wires per 1 μm

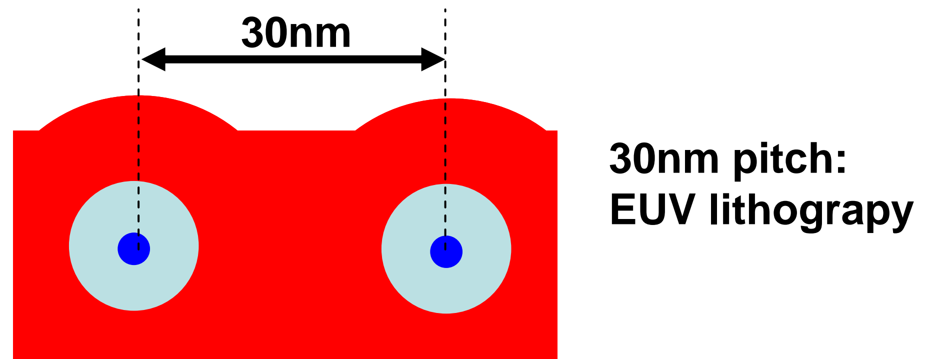
Front gate type MOS 165 wires /μm

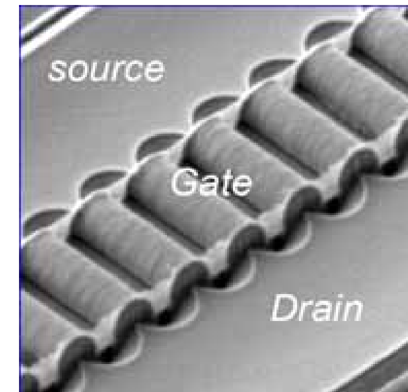


Surrounded gate type MOS 33 wires/μm



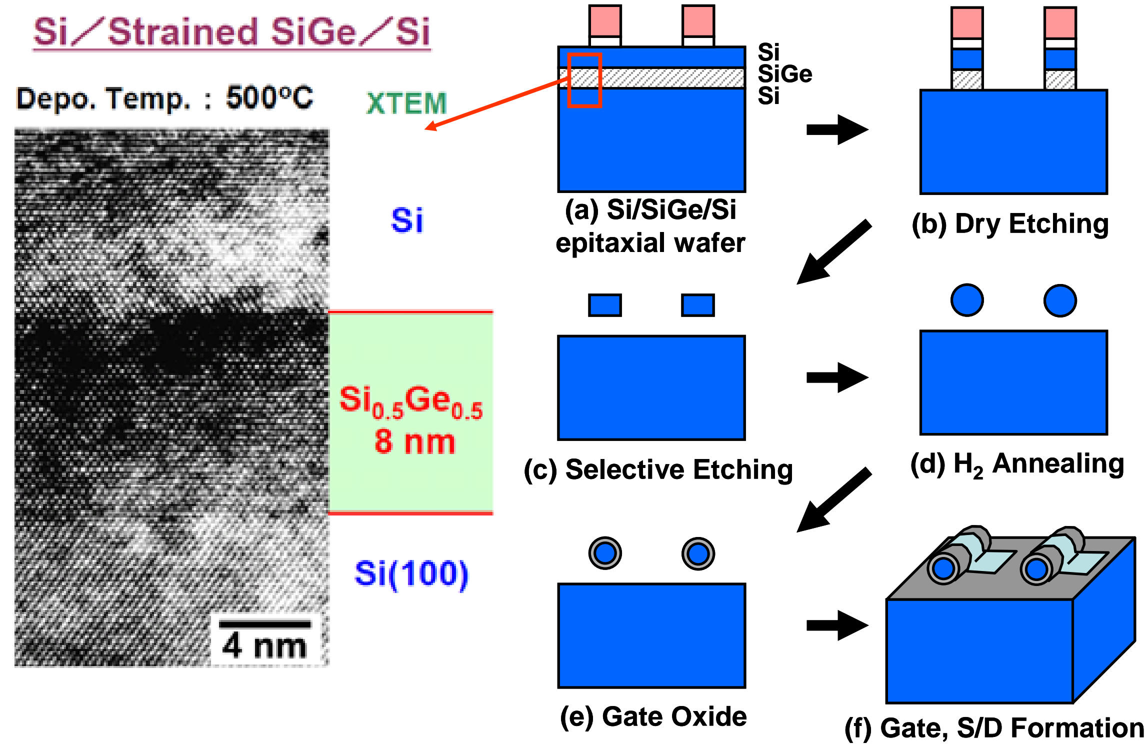


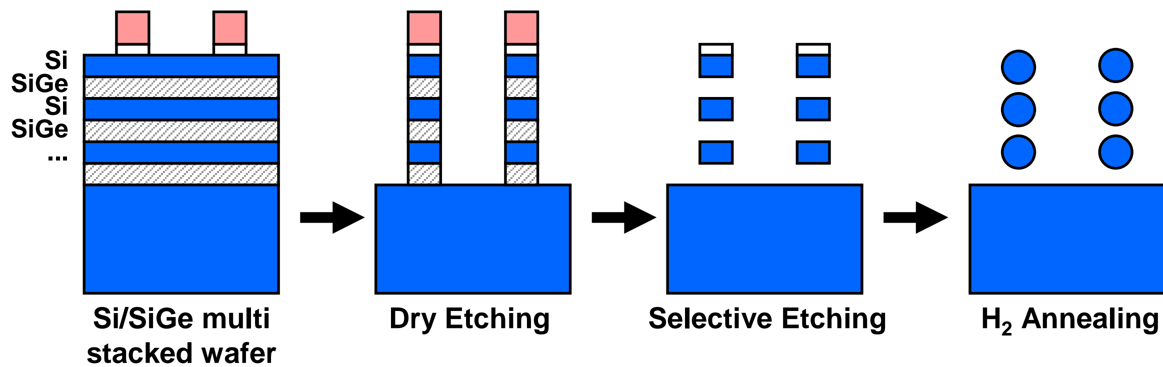




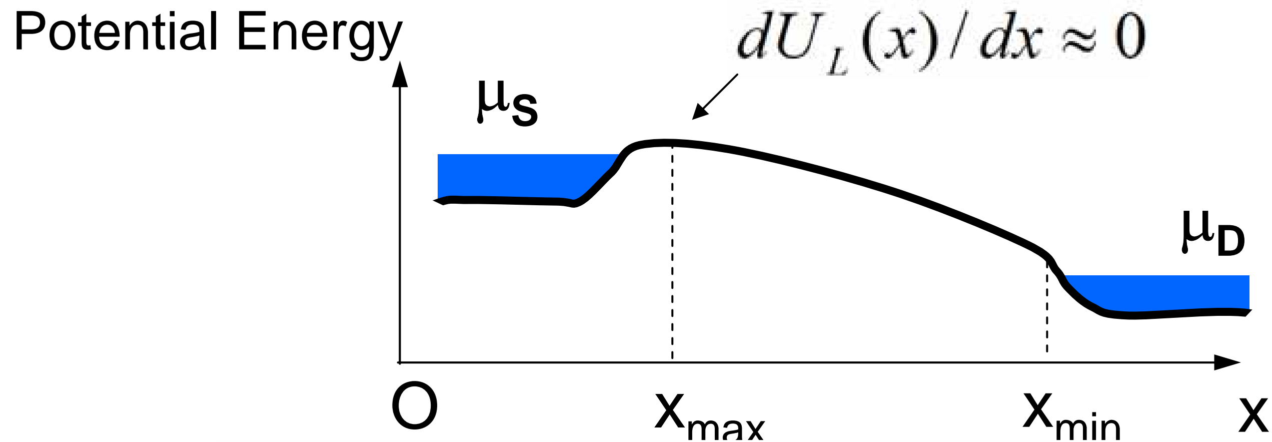
Surrounded gate MOS

Increase the number of wires towards vertical dimension





Landauer Formalism for Ballistic FET

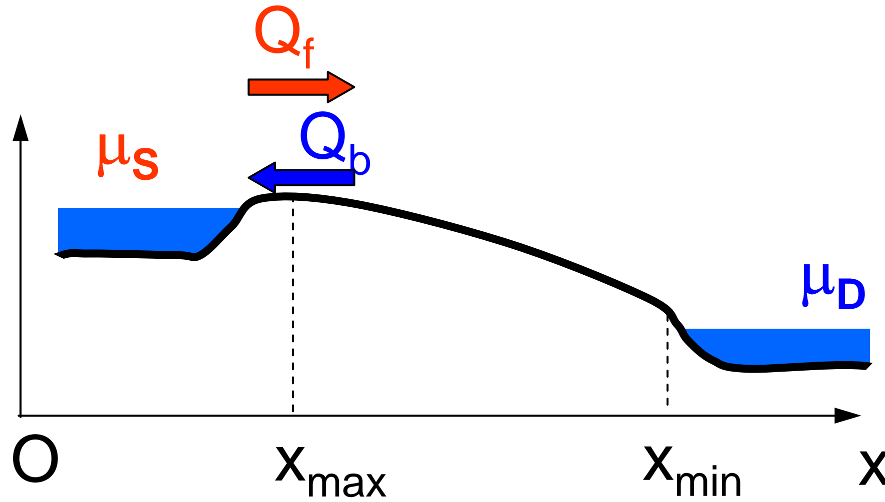


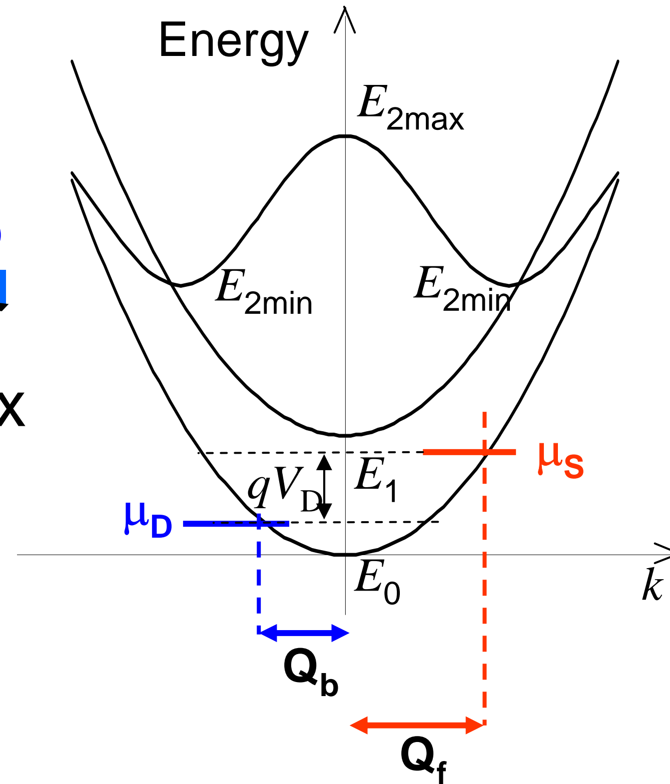
$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f(E,\mu_S) - f(E,\mu_D) \right] T_i(E)\, dE$$

From x_{max} to x_{min} $\quad T_i(E) \approx 1$

$$I_D = G_0 \left(\frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1 + \exp\left[(\mu_S - E_{i0}) / k_B T \right]}{1 + \exp\left[(\mu_D - E_{i0}) / k_B T \right]} \right\}$$

Carrier Density obtained from E-k Band

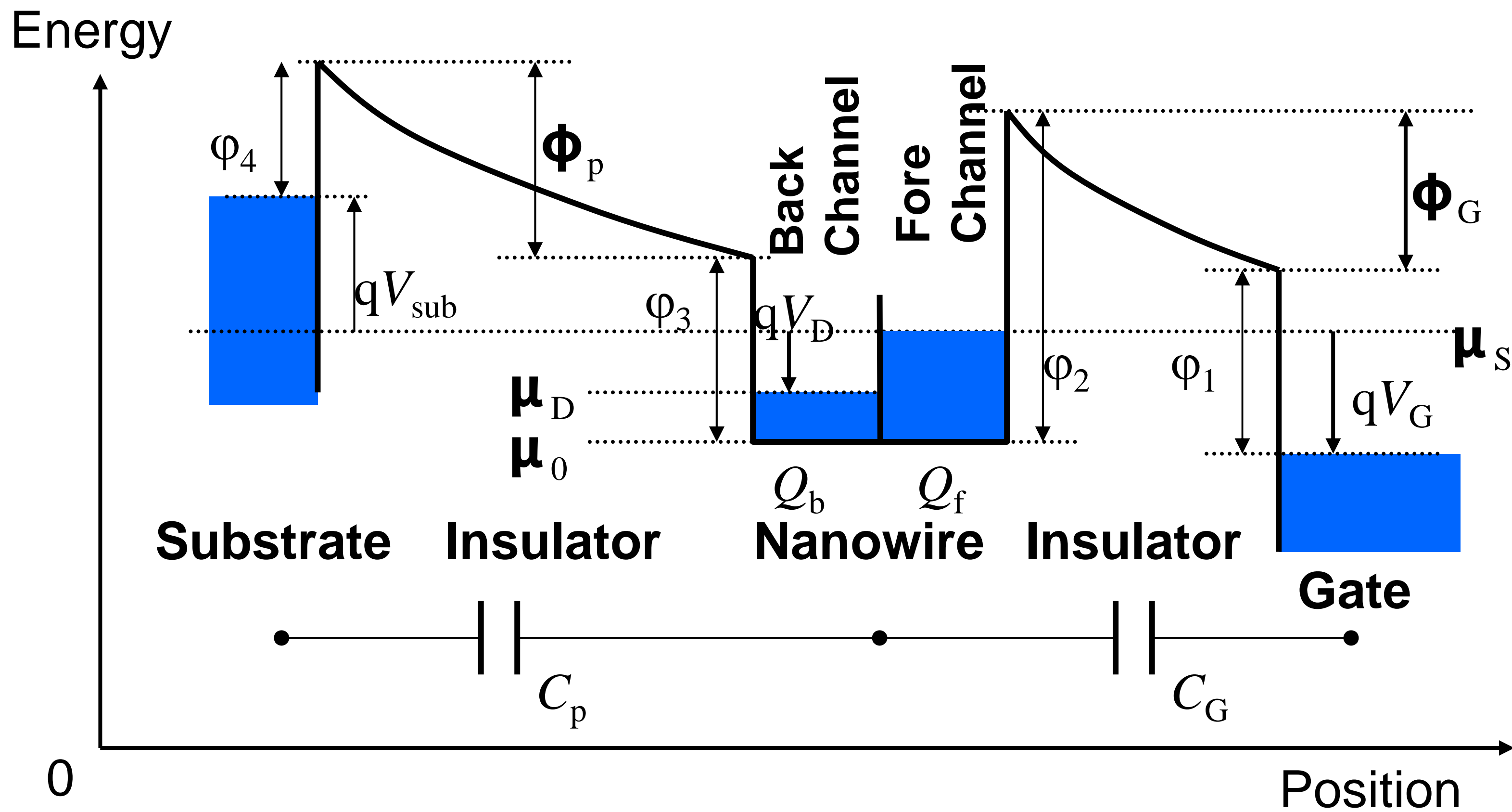




$$|Q| = |Q_f| + |Q_b|$$

$$= \frac{q}{\pi}\sum_i g_i \left[\int_{k_{i\min}}^{\infty} \frac{dk}{1+\exp\left\{\frac{E_i(k)-\mu_S}{k_B T}\right\}} + \int_{-\infty}^{k_{i\min}} \frac{dk}{1+\exp\left\{\frac{E_i(k)-\mu_D}{k_B T}\right\}} \right]$$

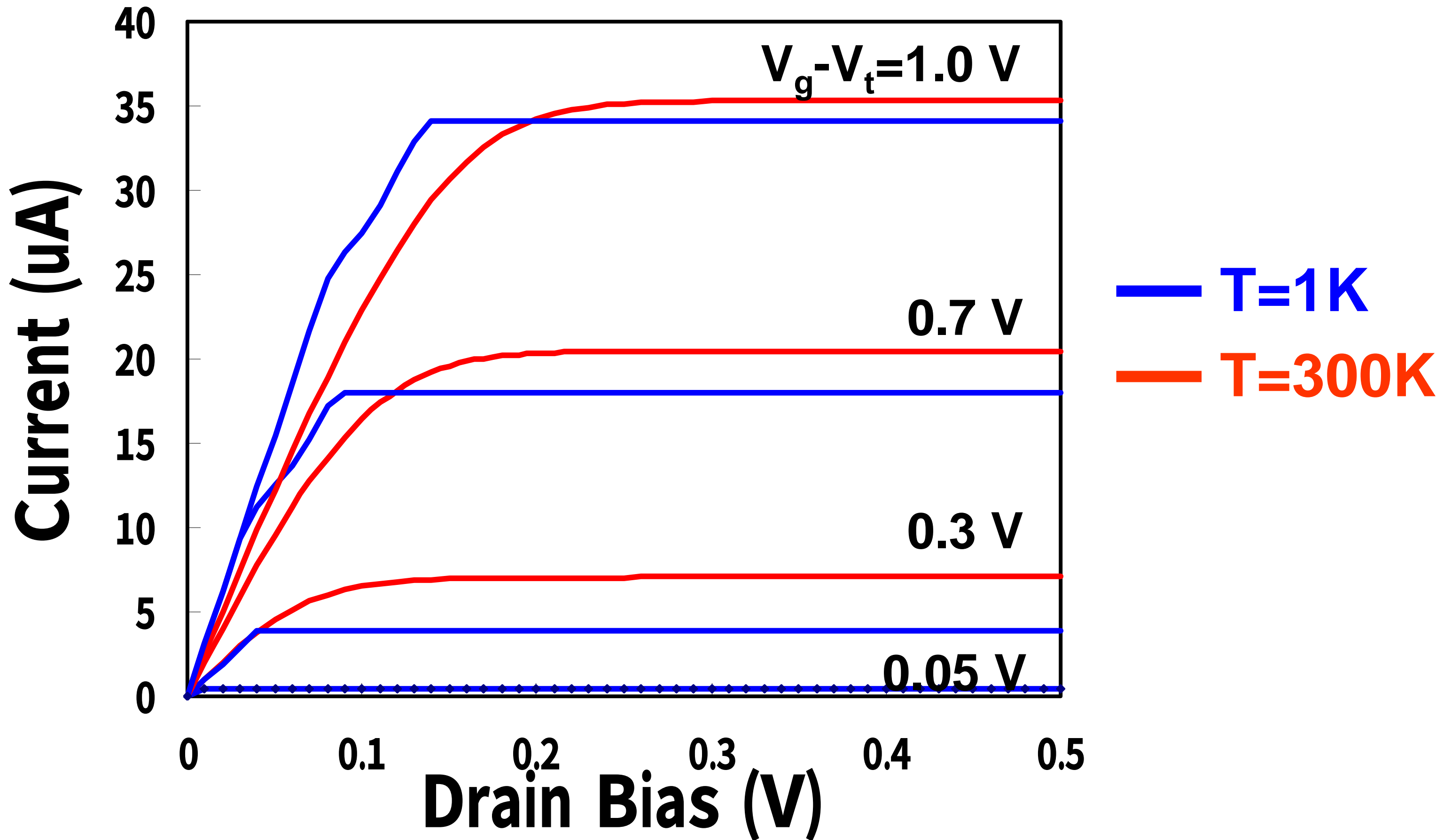
Carrier Density obtained from Band Diagram



$$\frac{|Q|}{C_G} = (V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q}$$

$$\alpha = 1 + \frac{C_P}{C_G}$$

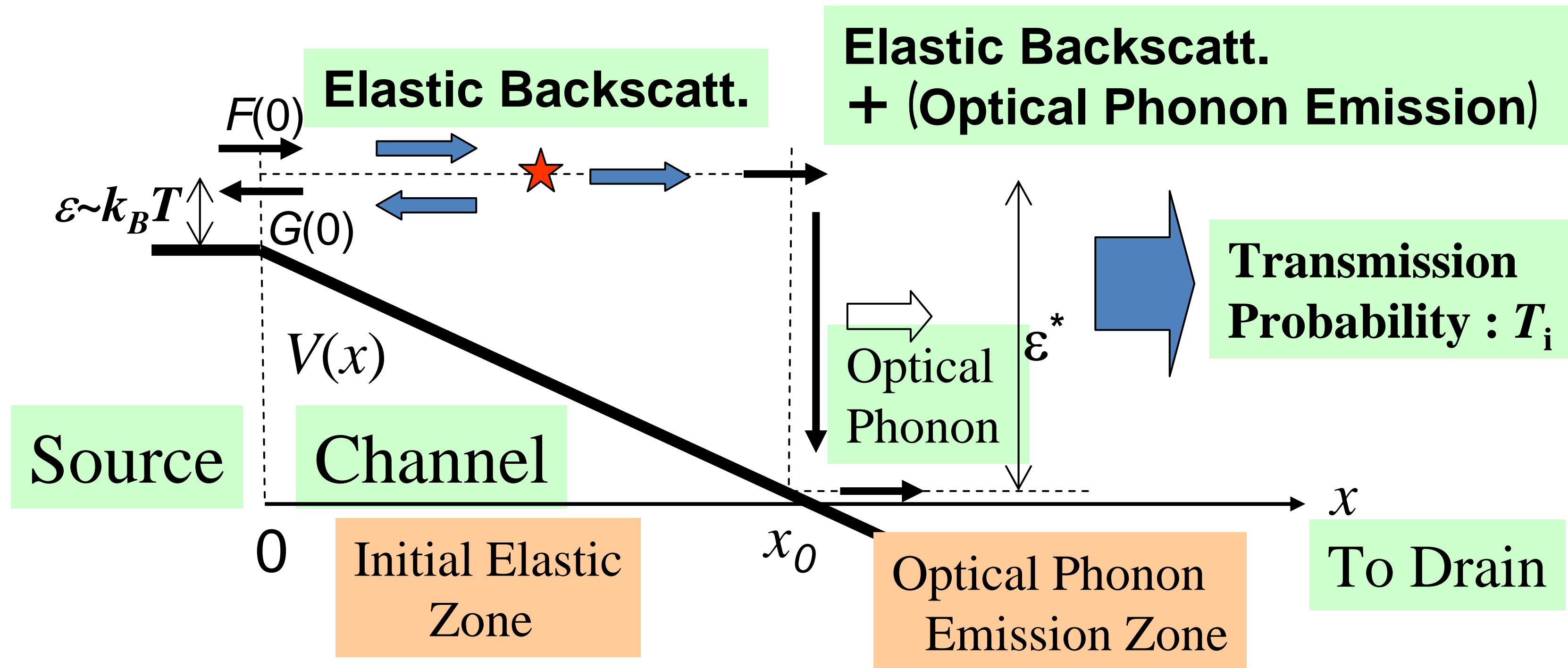
IV Characteristics of Ballistic SiNW FET



Small temperature dependency
35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx.： Electric Field E



Transmission Probability to Drain

$$T(\varepsilon) = \left.\frac{F(0) - G(0)}{F(0)}\right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I = \frac{q}{\pi\hbar}\sum_i g_i \int \left[f(\varepsilon,\mu_s) - f(\varepsilon,\mu_D) \right] T_i \, d\varepsilon$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left\{\frac{\sqrt{2r+t_{ox}}+\sqrt{t_{ox}}}{\sqrt{2r+t_{ox}}-\sqrt{t_{ox}}}\right\}}.$$

Planar Gate

$$(V_G - V_t) - \alpha\frac{\mu_S - \mu_0}{q} = \frac{|Q_f + Q_b|}{C_G}.$$

$$\mu_S - \mu_D = qV_D$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left(\frac{r+t_{ox}}{r}\right)}.$$

GAA

(Electrostatics requirement)

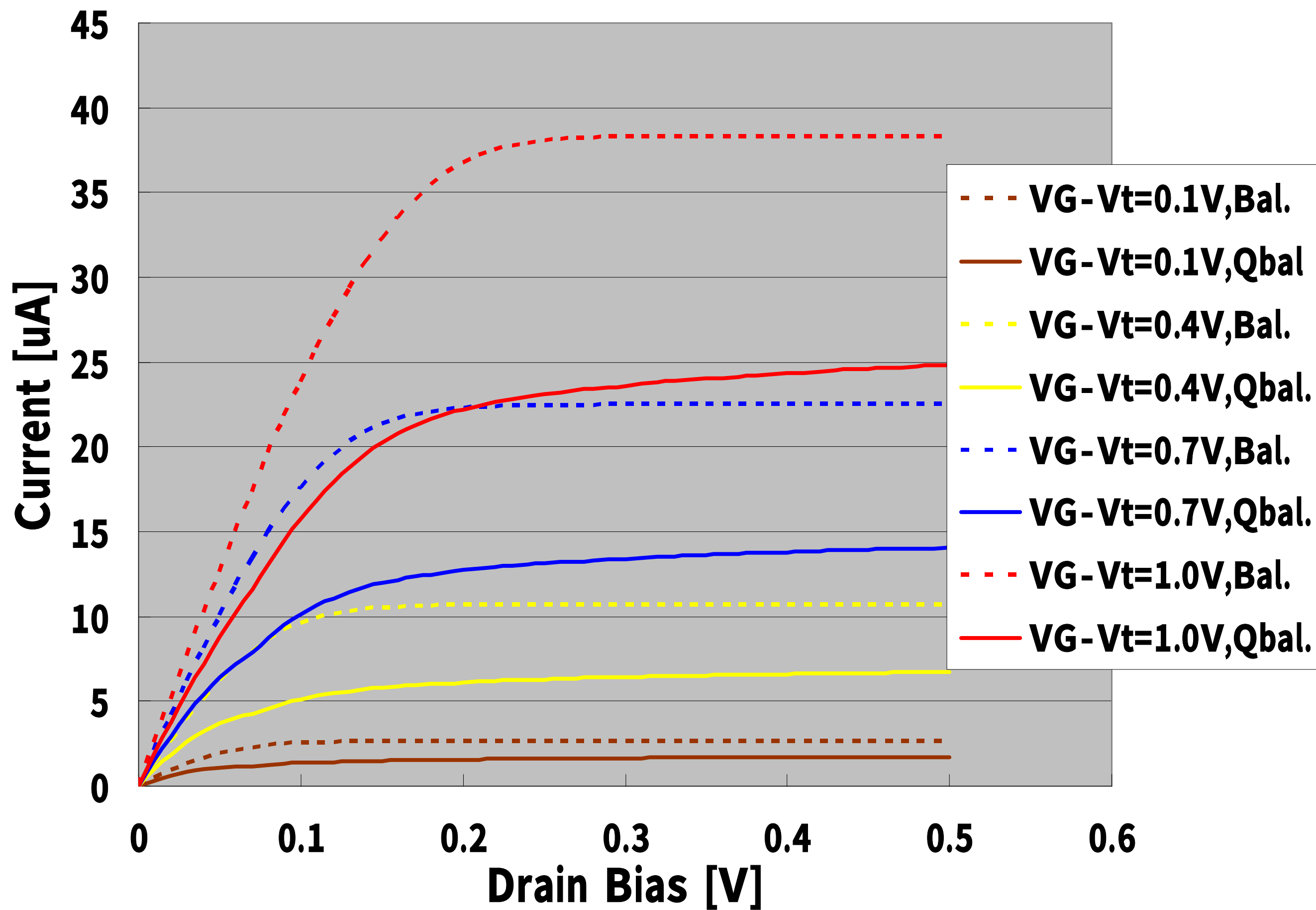
$$|Q_f + Q_b| = \frac{q}{\pi}\sum_i g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1+\exp\left\{\frac{\varepsilon_i(k)-\mu_S}{k_B T}\right\}} - \int_{-\infty}^{0} \left\{ \frac{1}{1+\exp\left\{\frac{\varepsilon_i(k)-\mu_S}{k_B T}\right\}} - \frac{1}{1+\exp\left\{\frac{\varepsilon_i(k)-\mu_D}{k_B T}\right\}} \right\} T_i(\varepsilon_i(k))\, dk \right]$$

$$T(\varepsilon) = \frac{\sqrt{2D_0}\, qE}{\left(\sqrt{B_0 + D_0} + \sqrt{D_0}\right) qE + \sqrt{2mD_0}\, B_0 \ln\left(\frac{qEx_0 + \varepsilon}{\varepsilon}\right)}$$

(Carrier distribution in Subbands)

Unknowns are I_D, $(\mu_S - \mu_0)$, $(\mu_D - \mu_0)$, および $(Q_f + Q_b)$

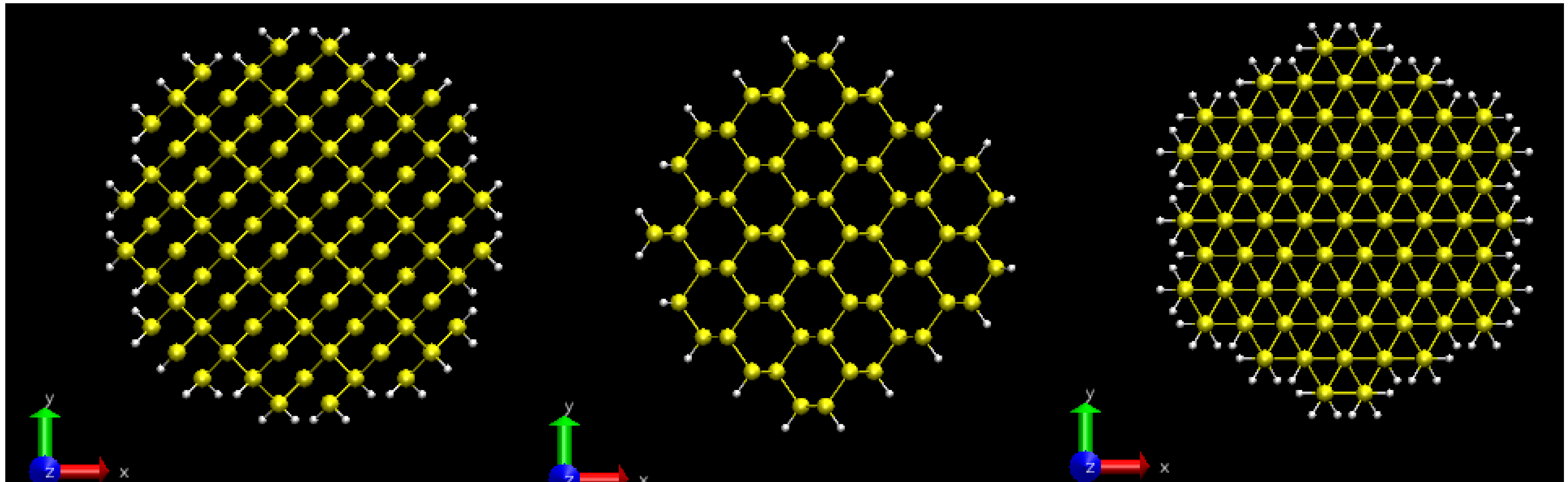
I-V_D Characteritics (RT)



- Electric current 20〜25 μA
- No satruration at Large V_D

Cross section of Si NW

First principal calculation, TAPP

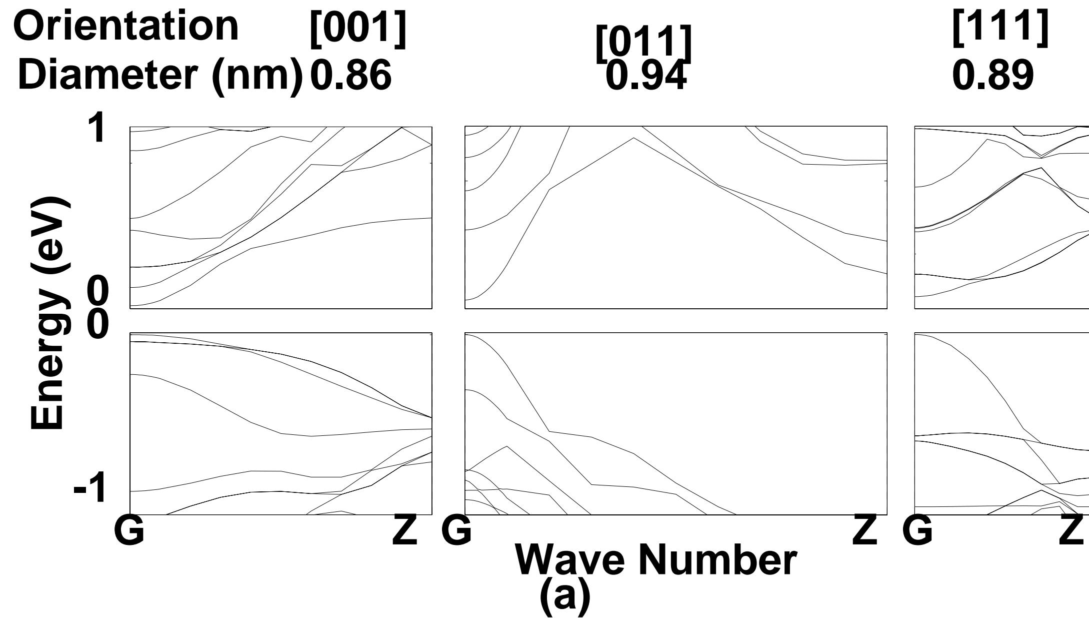


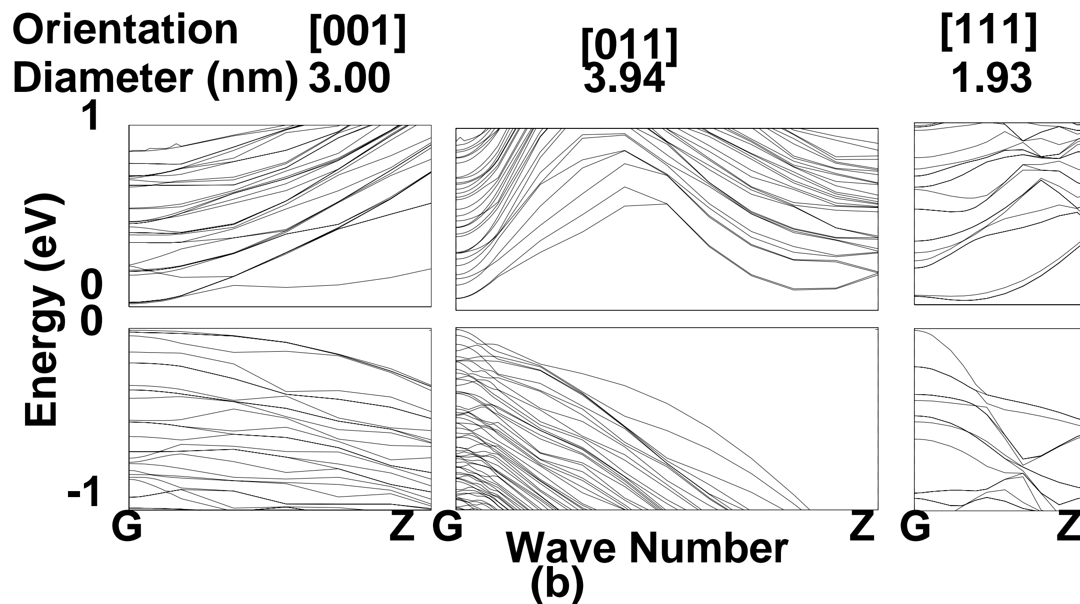
D=1.96nm [001]

D=1.94nm [011]

D=1.93nm [111]

Si nanowire FET with 1D Transport



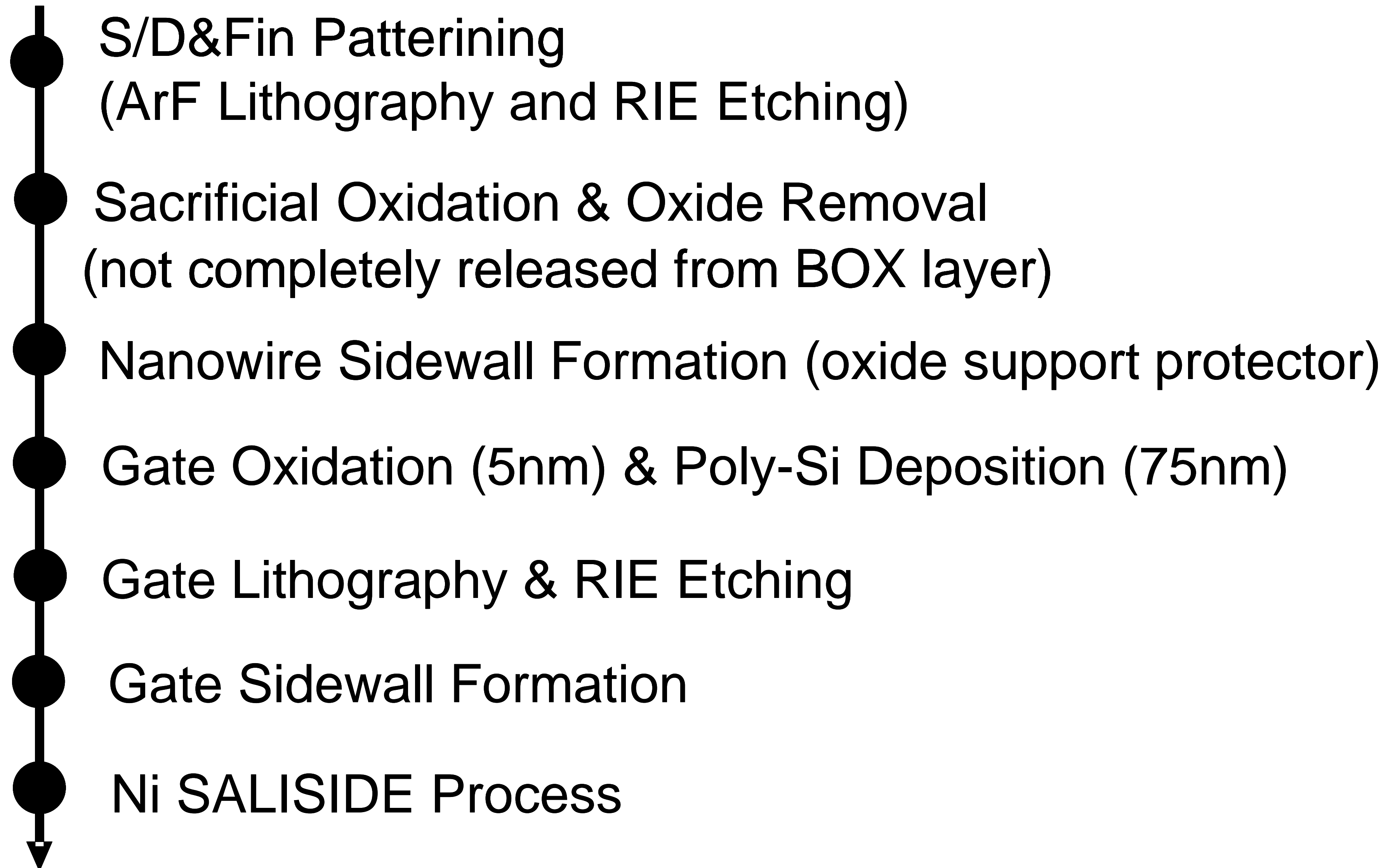


Small mass with [011]

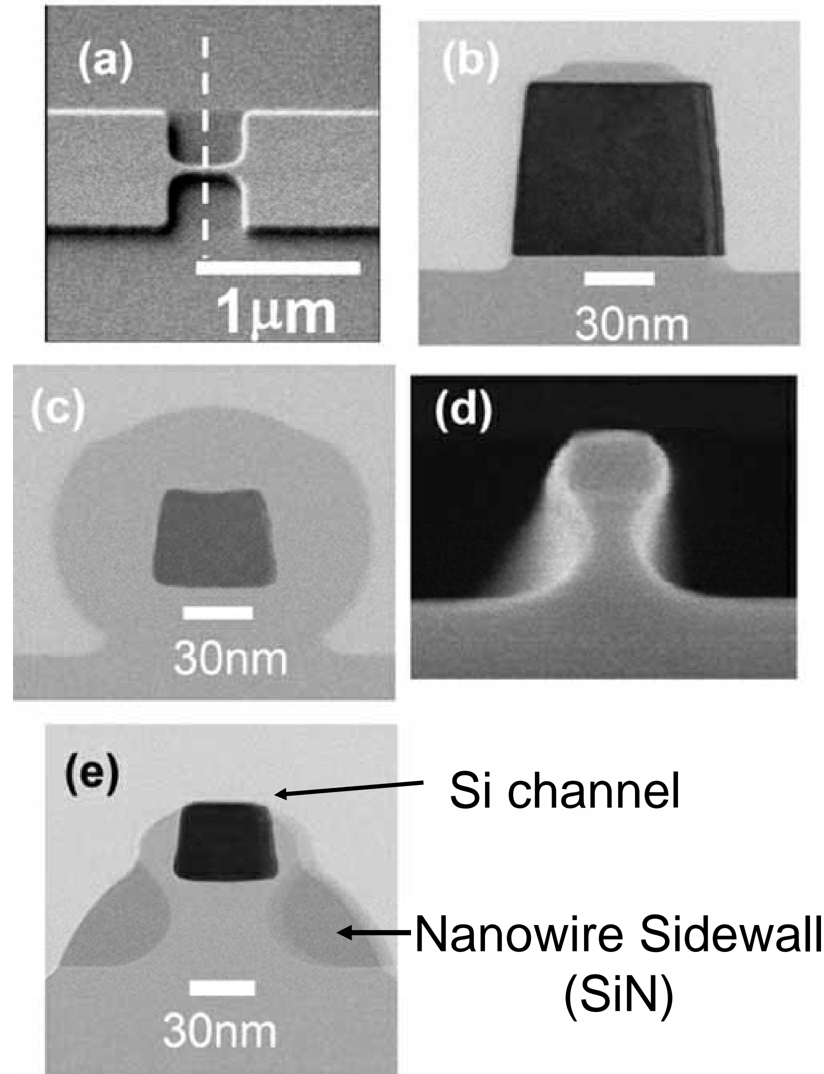
Large number of quantum channels with [001]

SiNW FET Fabrication

Brief process flow of Si Nanowire FET

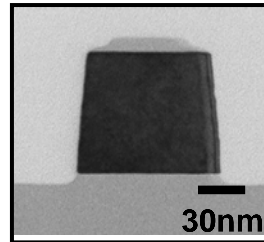


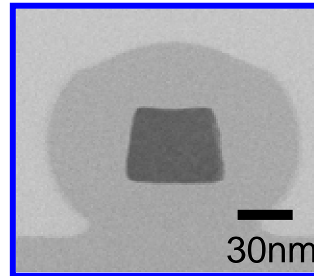
(a) Fin structure formed on BOX layer. (b)XTEM image of fin shown in (a) (c) XTEM image after sacrificial oxidation (d) Cross sectional SEM image after partial removal of sacrificial oxide (e) XTEM after nanowire sidewall formation

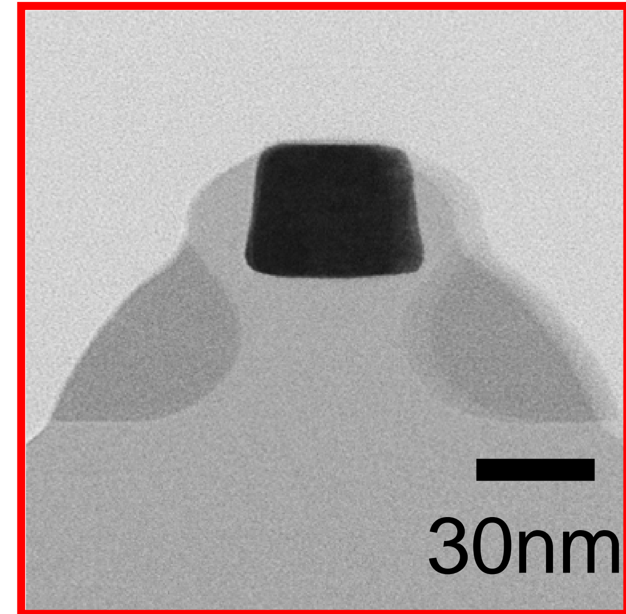


SiNW FET Fabrication

- S/D & Fin Patterning
- Sacrificial Oxidation
- Oixde etch back
- SiN sidewall support formation
- Gate Oxidation & Poly-Si Deposition
- Gate Lithography & RIE Etching
- Gate Sidewall Formation
- Ni SALISIDE Process (Ni 9nm / TiN 10nm)
- Backend

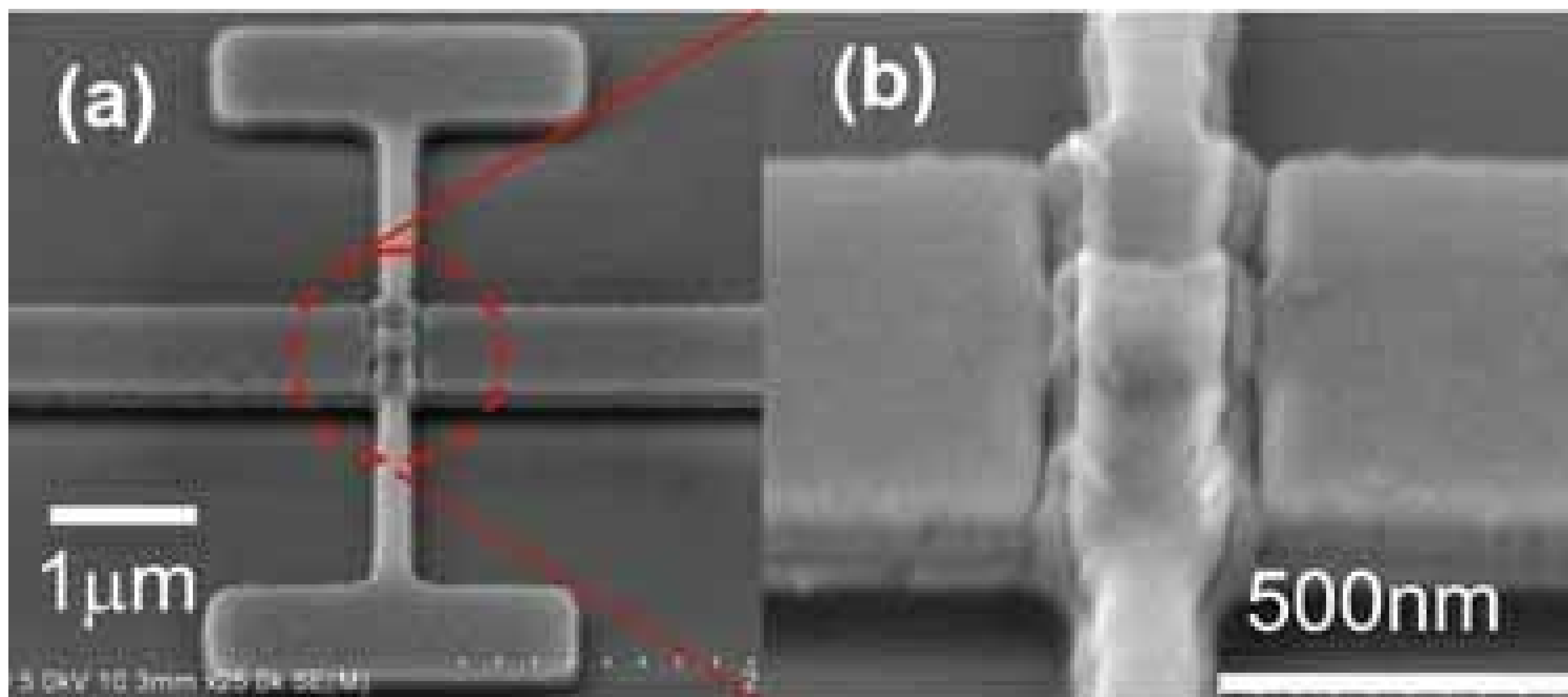




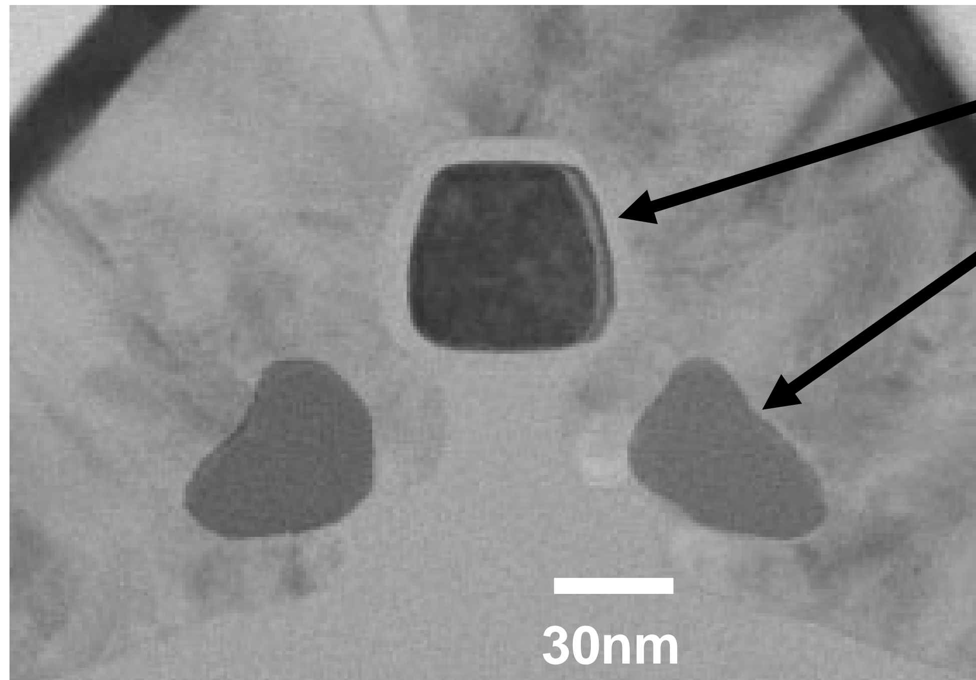


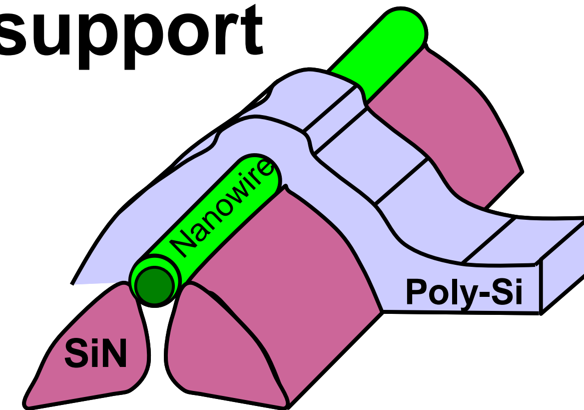
Standard recipe for gate stack formation

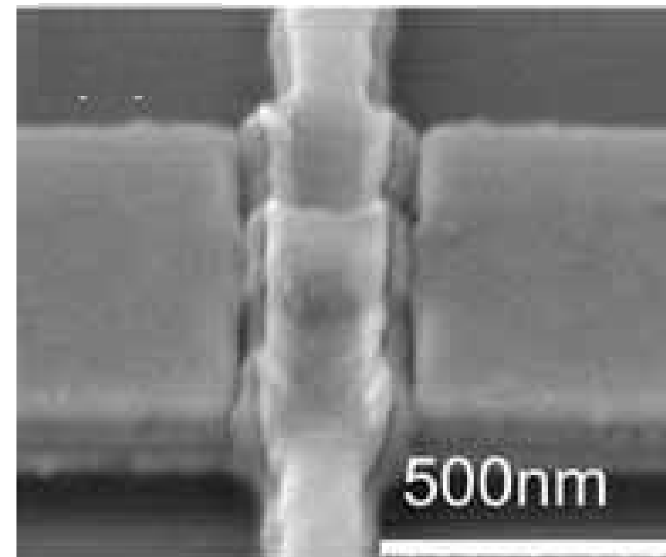
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.



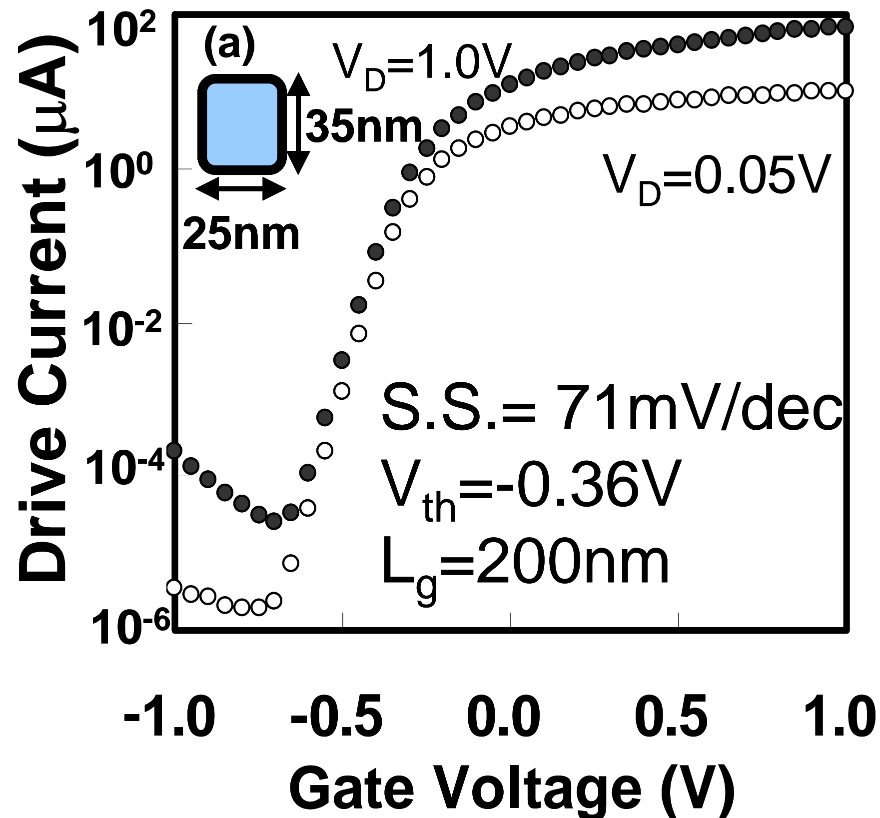
Fabricated SiNW FET

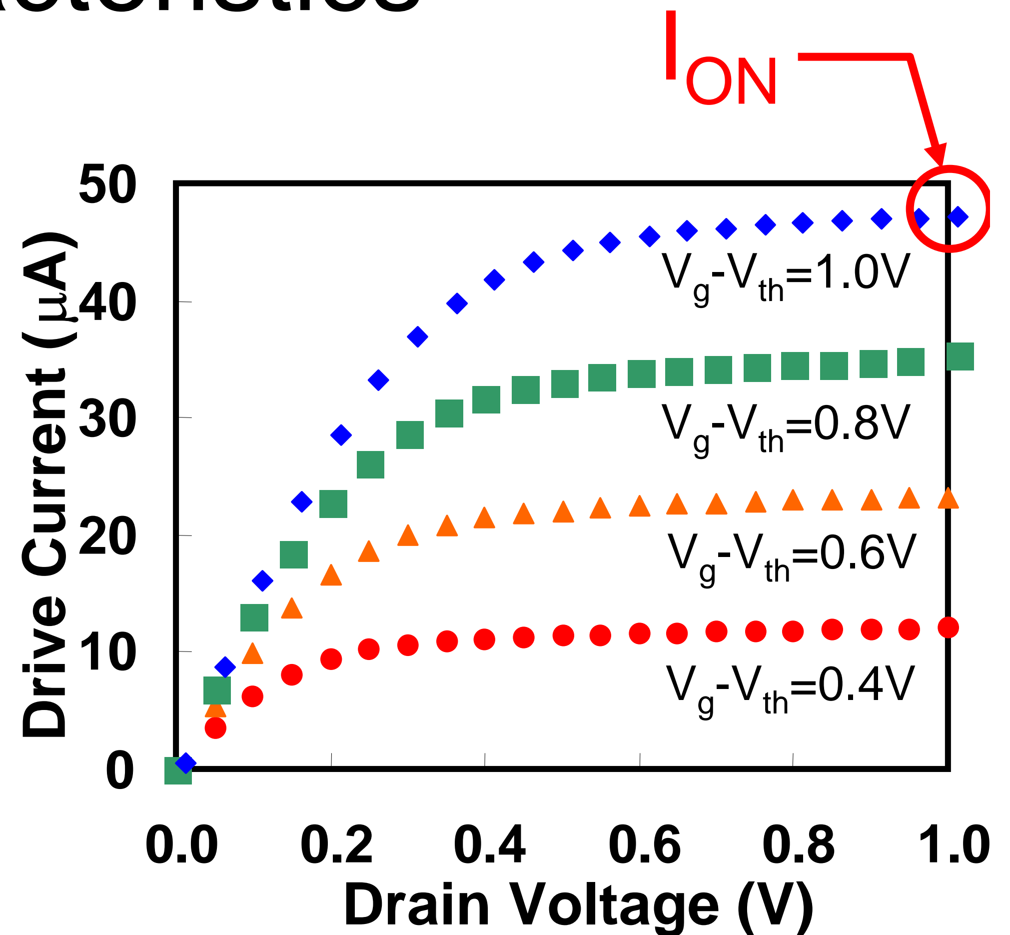






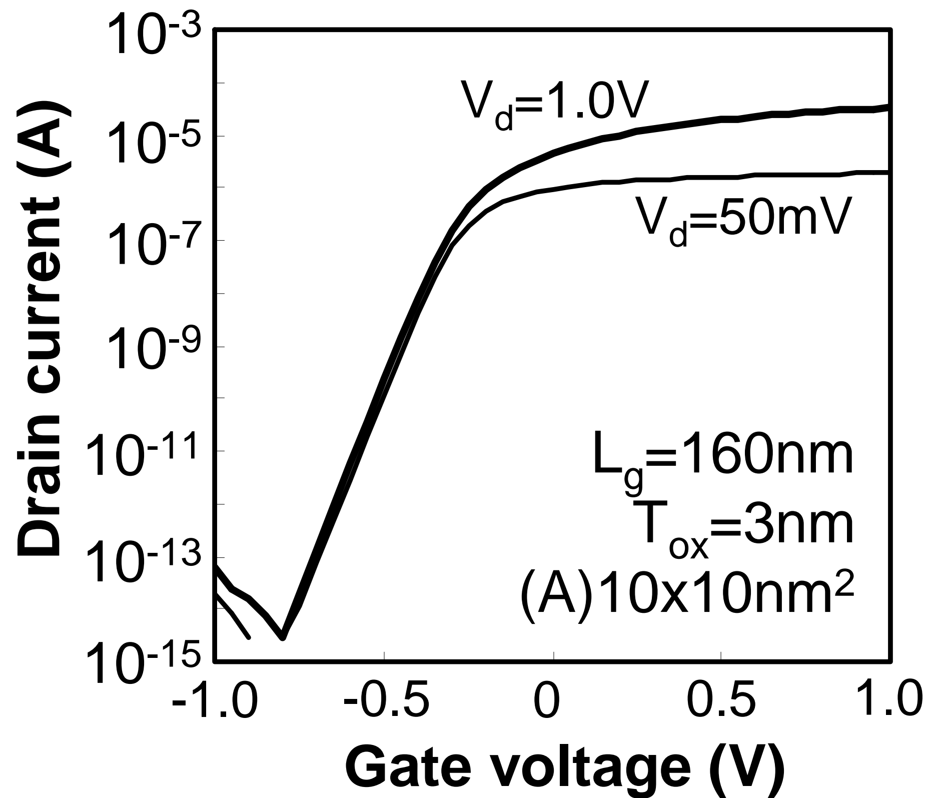
I_dV_g and I_dV_d Characteristics

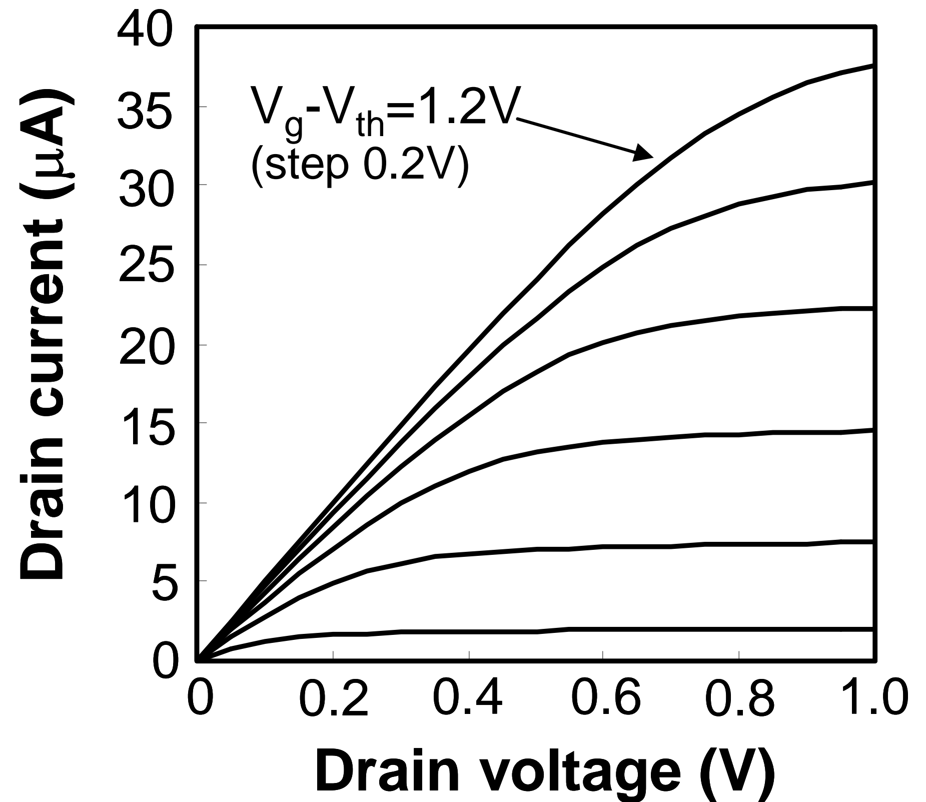




I_{on}/I_{off} ratio of ~10^7, high I_{on} of 49.6 μA/wire

Output characteristics of 10x10cm^2 SiNW FET





Our roadmap for R &D

Source: H. Iwai, IWJT 2008

2007 2010 2015 2020 2025 2030 2035

Extended CMOS: More Moore + CMOS logic

Research
Developmen
Production

PJT(2007~2012)

Beyond the horizon

Si Channel

Si Fin, Tri-gate

Natural direction of downsizing

Si Nano wire

Mechanical Stress, Roughness, Surface control

III-Vand Ge Nano wire

Nanowire

Selection

Problem: High-k gate oxides, etching of III-V wire

Selection

Tube

CNT

Tube, Ribbon

Selection

Ribbon

Graphene

ITRS

ITRS Beyond CMOS

High conduction By 1D conduction

Cloud

Horizon

More Moore

Extended CMOS More Moore ??

Current Issues

Si Nanowire

Control of wire surface property
Source Drain contact
Optimization of wire diameter
Compact I-V model

III-V & Ge Nanowire

High-k gate insulator
Wire formation technique

CNT:

Growth and integration of CNT
Width and Chirality control
Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique
Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

Thank you for your attgengtion